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09/777,954	02/07/2001	Hideaki Minamide	401073	5794

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EXAMINER	
KISS, ERIC B	

ART UNIT	PAPER NUMBER
2122	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,954	MINAMIDE ET AL.	
	Examiner	Art Unit	
	Eric B. Kiss	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-32 have been examined.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement filed February 7, 2001, fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because each publication listed in an information disclosure statement must be identified by publisher, author (if any), title, relevant pages of the publication, date, and place of publication (see 37 CFR 1.98(b)(5). It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Oath/Declaration

4. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> It does not state that the person making the oath or declaration acknowledges the duty to disclose to the Office all information known to the person to be material to patentability as defined in 37 CFR 1.56.

Applicant has only acknowledged the duty to disclose information under 37 CFR 1.56**(a)**. The duty to disclose information under 37 CFR 1.56, in its entirety (including 37 CFR 1.56(a-e)), must be acknowledged.

Specification

5. The disclosure is objected to because of the following informalities:

On p. 2 of the Preliminary Amendment filed February 7, 2001, Applicant's instruction to, "Replace the paragraph beginning at page 4, line 20..." appears to have been made in error. The wording of the supplied replacement paragraph instead appears to have been more appropriate for the paragraph beginning at page, line 11. A new amendment to the specification should be provided appropriately replacing both of the aforementioned paragraphs.

Appropriate correction is required.

6. It is noted that Applicant's preliminary amendment filed February 7, 2001, has been entered **in part**. The following is a summary of those portions of the preliminary amendment that have not been entered:

Applicant's amendments to the Abstract of the Disclosure have not been entered because they are not in compliance with 37 CFR §1.121.

Applicant's first instruction to "Replace the paragraph beginning at page 28, line 2," has not been entered because it appears to have been made in error. The replacement text provided is a duplicate of the replacement text from the immediately prior instruction. Additionally, the immediately following instruction replaces the same paragraph.

Claim Objections

7. Claim 9 is objected to because of the following informalities: "constitutes" in line 6 should presumably read --constituting--. Appropriate correction is required.

8. Claim 17 is objected to because of the following informalities: "Is" in line 5 should not be capitalized. Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claims 1-4, 6, 13-19, and 25-32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claims 1, 2, 6, 12, 13, 19, and 25-32 the phrases "universal microprocessor" and "universal computer" are not sufficiently defined in the specification or in the prior art to the extent necessary for one of ordinary skill in the art to make and use the described invention within any reasonable level of experimentation. In the interest of compact prosecution, the Examiner subsequently ignores all occurrences of the word "universal" in the claims for the purpose of further examination.

Claims 3, 4, and 14-18 are rejected based on limitations recited in their respective parent claims and rejected as set forth above.

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1-19 and 22-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 2, 5, 6, 12, 13, 19, 22-32, the phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d). In the interest of compact prosecution, the Examiner presumes the phrases following each recitation of "such as" are optional interpretations of the affected limitations and accordingly, these phrases are subsequently ignored for the purpose of further examination.

Further, regarding claims 12, 19, 27, and 28, it is unclear what meaning Applicant assigns to the terms "advanced programming language" and "advanced language". Although the instant specification provides an enabling example of such an "advanced programming language", i.e., the C programming language, it is unclear how other programming languages would be included or excluded by the unspecified "advanced programming language" criteria. Accordingly, these terms render the affected claims indefinite. In the interest of compact prosecution, the Examiner subsequently interprets "advanced programming language" and "advanced language" to mean any known programming language for the purpose of further examination.

Claims 3, 4, 7-11, and 14-18 are rejected based on limitations recited in their respective parent claims and rejected as set forth above.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,594,917 to Palermo et al.

As per claim 1, Palermo et al. disclose a programmable controller that performs sequential processing in accordance with execution codes generated by compiling a control program (see, for example, the Abstract; and col. 2, line 53, through col. 3, line 17), said programmable controller comprising: a storing unit which stores the execution codes (see, for example, col. 2, line 53, through col. 3, line 17); and a microprocessor including an acceleration unit (see, for example, col. 2, line 53, through col. 3, line 17), and directly executing the execution codes (see, for example, col. 2, line 53, through col. 3, line 17).

15. Claims 1, 2, 4-9, 11-16, 18, 21, 22, 25-27, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Hyung Seok Kim, et al., "A Translation Method of Ladder Diagram on PLC with Application to a Manufacturing Process," 1999 (hereinafter [Kim99]).

As per claim 1, [Kim99] discloses a programmable controller that performs sequential processing in accordance with execution codes generated by compiling a control program (see, for example, section 3 on pp. 2-4), said programmable controller comprising: a storing unit which stores the execution codes (see, for example, section 3 on pp. 2-4); and a microprocessor

including an acceleration unit (see, for example, section 3 on pp. 2-4), and directly executing the execution codes (see, for example, section 3 on pp. 2-4).

As per claim 2, [Kim99] discloses a control-program-development supporting apparatus that develops a control program described with a sequential-control language, said control-program-development supporting apparatus comprising a compiler which compiles the control program into codes directly executable by a microprocessor that includes an acceleration unit (see, for example, section 3 on pp. 2-4).

As per claim 4, [Kim99] further discloses a processing-time rough-estimating unit which has a relating table which relates a sample program having a known processing time with the control program corresponding to the execution codes to estimate sequential-processing execution time of a programmable controller in accordance with the relating table (see, for example, section 4 on pp. 4-5; the use of underlying apparatus components is inherent in determining the execution times of the modified programs as disclosed).

As per claim 5, [Kim99] discloses a control-program-development supporting apparatus that develops a control program described with a sequential-control language, said control-program-development supporting apparatus comprising: a control-program dividing unit which divides the control program into a plurality of blocks (see, for example, section 3 on pp. 2-4); and a compiler which compiles at least some of the blocks into execution codes directly executable by a programmable controller (see, for example, section 3 on pp. 2-4).

As per claim 6, [Kim99] further discloses the programmable controller including a microprocessor having an acceleration unit (see, for example, section 3.2 on p. 4).

As per claim 7, [Kim99] further discloses the control program being a ladder logic diagram or an instruction list generated from the ladder diagram, and the control-program dividing unit dividing the control program into a plurality of blocks at a predetermined rung in the ladder diagram to generate a program file for every block concerned (see, for example, section 3 on pp. 2-4).

As per claim 8, [Kim99] further discloses the control program being a ladder diagram or an instruction list generated from the ladder diagram, and the control-program dividing unit dividing the control program into a plurality of blocks at a predetermined rung serving as a jump destination for a jump instruction in the ladder diagram to generate a program file for every block (see, for example, section 3 on pp. 2-4).

As per claim 9, [Kim99] further discloses the control-program being a ladder diagram or an instruction list generated from the ladder diagram, and the control-program dividing unit extracting at least some rungs including instruction to a common input or output device from the ladder diagram, constituting one block of at least some of the rungs extracted, and generating a program file for every block (see, for example, section 3 on pp. 2-4).

As per claim 11, [Kim99] further discloses a processing-time rough-estimating unit which has a relating table which relates a sample program having a known processing time with the control program corresponding to the execution codes to estimate sequential-processing execution time of a programmable controller in accordance with the relating table (see, for example, section 4 on pp. 4-5; the use of underlying apparatus components is inherent in determining the execution times of the modified programs as disclosed).

As per claim 12, [Kim99] discloses a control-program-development supporting apparatus that develops a control program described with a sequential-control language, said control-program-program-development supporting apparatus comprising: a control-program dividing unit which divides the control program into a plurality of blocks (see, for example, section 3 on pp. 2-4); a control-program converting unit which converts at least some of the blocks into advanced-language control programs described with a computer-readable advanced language for every block (see, for example, section 3 on pp. 2-4); and a compiler which compiles at least some of the computer-readable advanced programming languages corresponding to every block into codes directly executable by a programmable controller (see, for example, section 3 on pp. 2-4).

As per claims 13-16 and 18, see the disclosure applied above to claims 6-9 and 11, respectively.

As per claim 21, [Kim99] discloses a storing unit which stores the execution codes; and a microprocessor for directly executing the execution codes, wherein the execution codes include binary data generated by compressing the control program (see, for example, section 3 on pp. 2-4; the code is optimized for length and execution time by the macrocompiler and the PLC-specific assembler reduces both the size of the memory and execution time required).

As per claim 22, [Kim 99] discloses a compressing unit which compresses the control program to generate a compressed file; a code converting unit which generates compressed data obtained by converting the compressed file into the code system of the control program; and a compiling unit which combines the control program with the compressed data and compiles the combined result into codes directly-executable by a programmable controller (see, for example,

section 3 on pp. 2-4; the code is optimized for length and execution time by the macrocompiler and the PLC-specific assembler reduces both the size of the memory and execution time required).

As per claim 25, [Kim99] discloses a storing unit which stores the execution codes; a microprocessor including an acceleration unit, and directly executing the execution codes (see, for example, section 3 on pp. 2-4); and a control-program-development supporting apparatus that develops a control program described with a sequential-control language, the control-program-development supporting apparatus having a compiler which compiles the control program into codes directly executable by a microprocessor that includes an acceleration unit (see, for example, section 3 on pp. 2-4).

As per claim 26, [Kim99] discloses a storing unit which stores the execution codes; a microprocessor which includes an acceleration unit and directly executing the execution codes (see, for example, section 3 on pp. 2-4); and a control-program-development supporting apparatus that develops a control program described with a sequential-control language, the control-program-development supporting apparatus having, a control-program dividing unit which divides the control program into a plurality of blocks (see, for example, section 3 on pp. 2-4); and a compiler which compiles at least some of the blocks into execution codes directly executable by a programmable controller (see, for example, section 3 on pp. 2-4).

As per claim 27, [Kim99] discloses a storing unit which stores the execution codes (see, for example, section 3 on pp. 2-4); a microprocessor which includes an acceleration unit and directly executing the execution codes (see, for example, section 3 on pp. 2-4); and a control-program-development supporting apparatus that develops a control program, described with a

sequential-control language, the control-program-development supporting apparatus having, a control-program dividing unit which divides the control-program into a plurality of blocks (see, for example, section 3 on pp. 2-4); a control-program converting unit which converts at least some of the blocks into advanced-language control programs described with a universal-computer-readable advanced language for every block (see, for example, section 3 on pp. 2-4); and a compiler which compiles at least some of universal-computer-readable advanced programming languages corresponding to every block into codes directly executable by a programmable controller (see, for example, section 3 on pp. 2-4).

As per claim 31, [Kim99] discloses a storing unit which stores the execution codes (see, for example, section 3 on pp. 2-4); and a microprocessor directly executing the execution codes, wherein the execution codes include binary data generated by compressing the control program (see, for example, section 3 on pp. 2-4; the code is optimized for length and execution time by the macrocompiler and the PLC-specific assembler reduces both the size of the memory and execution time required); and a control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, the control-program-development supporting apparatus having a compiler which compiles the control program into codes directly executable by a microprocessor that includes an acceleration unit (see, for example, section 3 on pp. 2-4).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 3, 10, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable [Kim99], as applied to claims 2, 5, and 12 above, in view of Alfred V. Aho, et al., "Compilers: Principles, Techniques, and Tools," 1988 (hereinafter [Aho88]).

As per claims 3, 10, and 17, in addition to the disclosure applied above to claims 2, 5, and 12, [Kim99] discloses an optimization filtering unit which reconstructs the control program into an optimum code system by rearranging codes for locally arranging instructions for a common input or output device, wherein a control program optimized by said optimization filtering unit is newly used as the control program (see, for example, section 3 on pp. 2-4). [Kim99] fails to expressly disclose excluding not-cited variables and redundant codes. However, [Aho88] teaches such well-known compiler optimization techniques as dead/redundant/unreachable code elimination (see, for example, section 9.9 on pp. 554-557; and section 10.2 on pp. 592-598). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the optimizing compiler framework disclosed by [Kim99] to

include such known optimization techniques as taught by [Aho88]. One would be motivated to do so to improve the quality of resulting generated code.

18. Claims 19 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable [Kim99] in view of Jonathan B. Rosenberg, "How Debuggers Work: Algorithms, Data Structures, and Architecture," 1996 (hereinafter [Ros96]).

As per claims 19 and 28, [Kim99] discloses a storing unit which stores execution codes (see, for example, section 3 on pp. 2-4); a microprocessor including an acceleration unit (see, for example, section 3.2 on p. 4) and directly executing the execution codes (see, for example, section 3 on pp. 2-4); and a control-program-development supporting apparatus that develops a control program described with a sequential-control language (see, for example, section 3 on pp. 2-4), having a control-program converting unit which converts a control program into an advanced-programming-language control program described with a computer-readable advanced programming language (see, for example, section 3 on pp. 2-4). [Kim99] fails to expressly disclose a debugging-code generating unit which generates a debugging control program by inserting a line number into a part corresponding to each line, constituting the instruction list in source codes, constituting the advanced-programming-language control program; and a debugging executing unit which displays each line of the instruction list and the execution part of the advanced-programming-language control program by relating the former with the latter. However, [Ros96] teaches that debuggers are critical tools for software development (see, for example, p. 1, line 1). [Ros96] further teaches that showing source code line correspondence is

part of the most important information the programmer needs during debugging, namely program context information (see, for example, "Context Is the Torch in a Dark Cave" on pp. 9-11) and that the developer of an application who is using a debugger has a lot to gain if the original source code is mapped directly to the application's machine code (see, for example, "Source-level (Symbolic) versus Machine-level" on p 12). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the system of [Kim99] to include such program code line number correspondence as per the teachings of [Ros96]. One would be motivated to do so to allow for efficient debugging of code under development.

19. Claims 20 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable [Kim99] in view of Brenda S. Baker, et al., "Compressing Differences of Executable Code," 1999 (hereinafter [Bak99]).

As per claims 20 and 30, [Kim99] discloses a programmable controller comprising a control-program-development supporting apparatus that develops a control program described with a sequential-control language, said control-program-development supporting apparatus comprising a compiler which compiles the control program into codes directly executable by a microprocessor that includes an acceleration unit (see, for example, section 3 on pp. 2-4); a first storing unit which stores the execution codes and a second storing unit for storing newly created execution code and a microprocessor for direct execution of the execution codes (see, for example, section 3 on pp. 2-4). [Kim99] fails to expressly disclose the second storing unit

storing data for the difference between an execution code stored in the first storing unit and a new execution code and a patch processing unit which changes an execution code currently executed into a new execution code at a predetermined timing in accordance with the difference data and continuously executing the changed execution code. However, [Bak99] teaches the use of patches that encode the differences between two versions of a program as one of the most common ways to deliver such changes (see, for example, the Abstract). [Bak99] further discloses the necessary mechanism by which such patches can be generated and applied (see, for example, section 2 on pp. 3-4 and section 3 on p. 4). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the system of [Kim99] to include such patching based on differences between an existing program and an updated program as per the teachings of [Bak99]. One would be motivated to do so to provide updates in an efficient manner by transmitting smaller files.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

21. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Eric B. Kiss whose telephone number is (703) 305-7737. The Examiner can normally be reached on Tue. - Fri., 7:30 am - 5:00 pm. The Examiner can also be reached on alternate Mondays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Tuan Dam, can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBK/EBK
May 13, 2004

TUAN DAM
SUPERVISORY PATENT EXAMINER